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Memory Products	

# 82HS641 82HS641A 82HS641B

## 64K-bit TTL bipolar PROM

### DESCRIPTION

The 82HS641, 82HS641A and 82HS641B are field-programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82HS641 devices are supplied with all outputs at logical High. Outputs are programmed to a logic Low level at any specified address by fusing the vertical junction matrix.

These devices include on-chip decoding with 1 Chip Enable input for ease of memory expansion. They feature 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Handbook.

### FEATURES

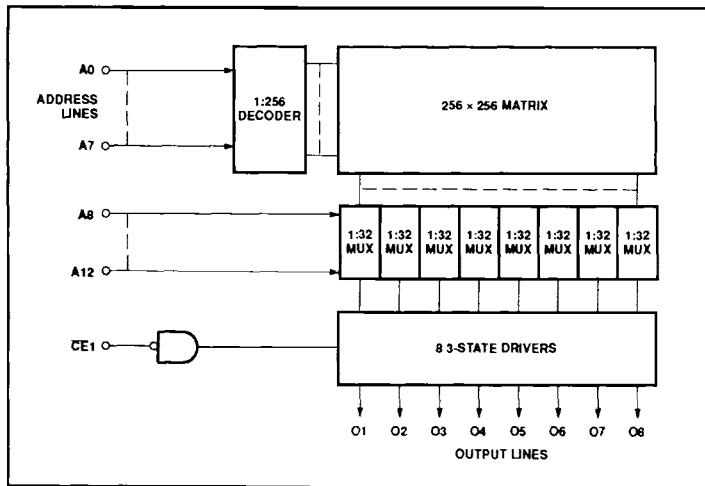
- Address access time:
  - N82HS641: 55ns max
  - N82HS641A: 45ns max
  - N82HS641B: 35ns max
- Power dissipation: 10μW/bit typ
- Input loading: -250μA max
- One Chip Enable input
- On-chip address decoding

- No separate fusing pins
- Unprogrammed outputs are High level
- Fully TTL compatible
- Outputs: 3-State

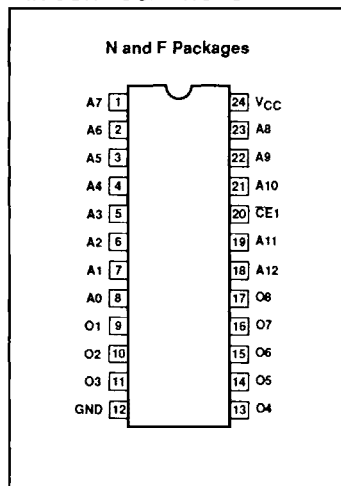
### APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

### BLOCK DIAGRAM



### PIN CONFIGURATIONS



# 64K-bit TTL bipolar PROM (8192 × 8)

## 82HS641 / 82HS641A / 82HS641B

### ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Plastic Dual-In-Line 600mil-wide	N82HS641 N, N82HS641A N, N82HS641B N
24-Pin Ceramic Dual-In-Line 600mil-wide	N82HS641 F, N82HS641A F, N82HS641B F

### ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	+7.0	$V_{DC}$
$V_{IN}$	Input voltage	+5.5	$V_{DC}$
$V_O$	Output voltage Off-State	+5.5	$V_{DC}$
$T_{amb}$	Operating temperature range	0 to +75	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

### DC ELECTRICAL CHARACTERISTICS

 $0^{\circ}\text{C} \leq T_{amb} \leq +75^{\circ}\text{C}, 4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$ 

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1,2</sup>	LIMITS			UNIT
			Min	Typ <sup>3</sup>	Max	
<b>Input voltage</b>						
$V_{IL}$	Low <sup>4</sup>	$I_{IN} = -18\text{mA}$	2.0		0.8	V
$V_{IH}$	High <sup>4</sup>					
$V_{IC}$	Clamp					
<b>Output voltage</b>						
$V_{OL}$	Low	$\overline{CE}1 = \text{Low}$ $I_{OUT} = 16\text{mA}$	2.4		0.5	V
$V_{OH}$	High	$I_{OUT} = -2.0\text{mA}$				
<b>Input current</b>						
$I_{IL}$	Low	$V_{IN} = 0.45\text{V}$			-250	$\mu\text{A}$
$I_{IH}$	High	$V_{IN} = 5.25\text{V}$			40	$\mu\text{A}$
<b>Output current</b>						
$I_{OZ}$	Hi-Z state	$\overline{CE}1 = \text{High}, V_{OUT} = 0.5\text{V}$	-15		-40	$\mu\text{A}$
$I_{OS}$	Short circuit <sup>5</sup>	$\overline{CE}1 = \text{High}, V_{OUT} = 5.25\text{V}$				
		$\overline{CE}1 = \text{Low}, V_{OUT} = 0\text{V}$				
<b>Supply current<sup>6</sup></b>						
$I_{CC}$		$V_{CC} = 5.25\text{V}$		130	175	$\text{mA}$
<b>Capacitance</b>						
$C_{IN}$	Input	$\overline{CE}1 = \text{High}, V_{CC} = 5.0\text{V}$ $V_{IN} = 2.0\text{V}$		5		$\text{pF}$
$C_{OUT}$	Output	$V_{OUT} = 2.0\text{V}$		8		$\text{pF}$

#### NOTES:

- Positive current is defined as into the terminal referenced.
- All voltages are with respect to network ground.
- Typical values are at  $V_{CC} = 5\text{V}$ ,  $T_{amb} = +25^{\circ}\text{C}$ .
- Measured with one output switching from a Logic "1" to a Logic "0".
- Duration of the short circuit should not exceed 1 second.
- Measured with all inputs grounded and all outputs open.

# 64K-bit TTL bipolar PROM (8192 × 8)

## 82HS641 / 82HS641A / 82HS641B

### AC ELECTRICAL CHARACTERISTICS

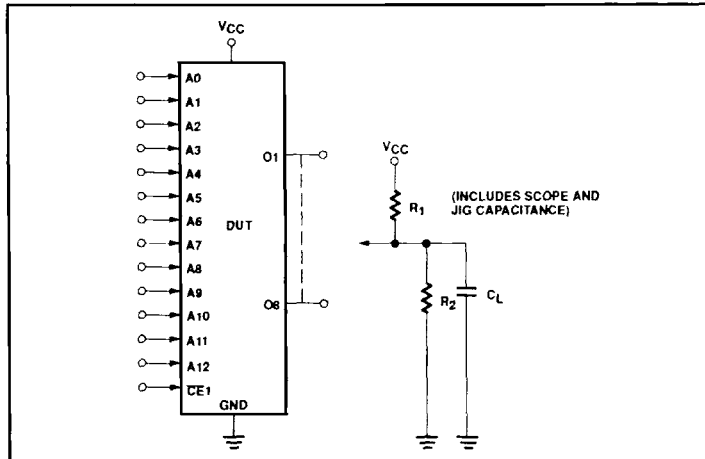
$R_1 = 270\Omega$ ,  $R_2 = 600\Omega$ ,  $C_L = 30\text{pF}$ ,  $0^\circ\text{C} \leq T_{\text{amb}} \leq +75^\circ\text{C}$ ,  $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$

SYMBOL	PARAMETER	TO	FROM	N82HS641			N82HS641A			N82HS641B			UNIT
				Min	Typ <sup>1</sup>	Max	Min	Typ <sup>1</sup>	Max	Min	Typ <sup>1</sup>	Max	
<b>Access time<sup>2</sup></b>													
$t_{AA}$		Output	Address		50	55		40	45		30	35	ns
$t_{CE}$		Output	Chip Enable		30	35		20	25		15	20	ns
<b>Disable time<sup>3</sup></b>													
$t_{CD}$		Output	Chip Disable		30	35		20	25		15	20	ns

**NOTES:**

1. Typical values are  $V_{\text{CC}} = 5\text{V}$ ,  $T_{\text{amb}} = +25^\circ\text{C}$ .
2. Tested at an address cycle time of  $1\mu\text{s}$ .
3. Measured at a delta of  $0.5\text{V}$  from Logic Level with  $R_1 = 750\Omega$ ,  $R_2 = 750\Omega$  and  $C_L = 5\text{pF}$ .

### TEST LOAD CIRCUIT



### VOLTAGE WAVEFORM

