

82S321 32K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S321 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S321 is supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

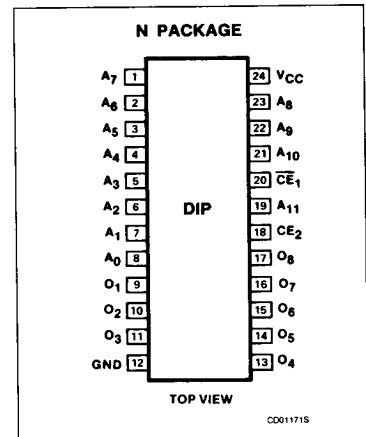
FEATURES

- Address access time: 70ns max
- Power dissipation: 20 μ W/bit typ
- Input loading: -100 μ A max
- Two chip enable inputs
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- Outputs: Three-state

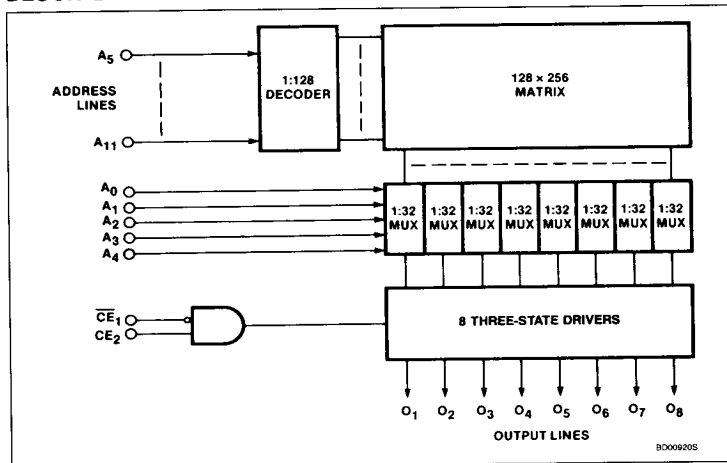
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



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32K-Bit TTL Bipolar PROM (4096 x 8)

82S321

ORDERING CODE

DESCRIPTION	ORDER CODES
Plastic Dual Inline 600mil wide 24-pin	N82S321 N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _O Output voltage Off-state	+5.5	V _{dc}
T _A Temperature range Operating	0 to +75	°C
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -12mA	2.0	-0.8	0.8 -1.2	V
Output voltage V _{OL} Low V _{OH} High	$\overline{CE}_1 = \text{Low}, CE_2 = \text{High}$ I _{OUT} = 9.6mA I _{OUT} = -2mA	2.4		0.45	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 40	μA
Output current I _{OZ} Hi-Z State I _{OS} Short circuit ³	$\overline{CE}_1 = \text{High}, CE_2 = \text{Low}, V_{OUT} = 0.5$ $\overline{CE}_1 = \text{High}, CE_2 = \text{Low}, V_{OUT} = 5.5$ $\overline{CE}_1 = \text{Low}, CE_2 = \text{High}, V_{OUT} = 0V$	-15		-40 40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25		130	175	mA
Capacitance C _{IN} Input C _{OUT} Output	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

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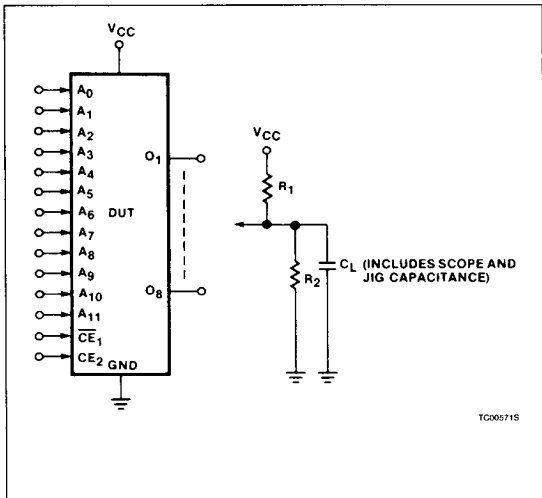
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ⁵	Max	
Access time⁴ T_{AA} T_{CE}	Output	Address Chip enable		60 20	70 25	ns
Disable time⁶ T_{CD}	Output	Chip disable		20	25	ns

NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μ sec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM

