

MB834000A-20

CMOS 4M-BIT MASK PROGRAMMABLE READ ONLY MEMORY

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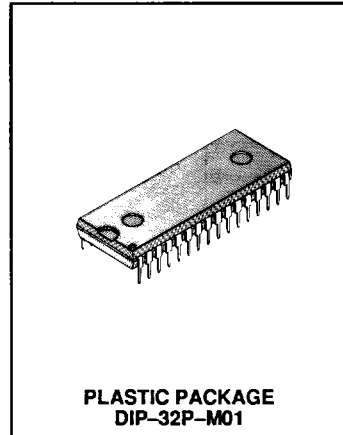
DESCRIPTION

The Fujitsu MB834000A is a CMOS Si-gate mask-programmable static read only memory organized as 524, 288 words by 8bits.

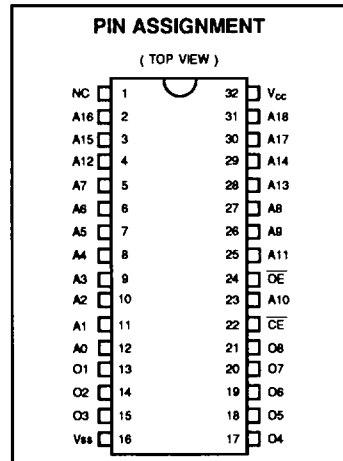
The MB834000A has TTL-compatible I/O 3-state output level with fully-static operation (i.e. no need of clock signal) and single +5V power supply.

Also, the MB834000A is designed for applications such as character generator or program strage which require large memory capacity and high-speed/low-power operation.

- Organization: 524, 288 word x 8bit
- Access time: 250ns max.
- Completely static operation: No clock required
- TTL compatible Input/Output
- Three state output
- Single +5V power supply
- Power dissipation: 220mW max. (Active)
5.5mW max. (Standby, TTL input level)
0.275mW max. (Standby, CMOS input level)
- 32-pin Plastic DIP: Suffix-P



PLASTIC PACKAGE
DIP-32P-M01



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

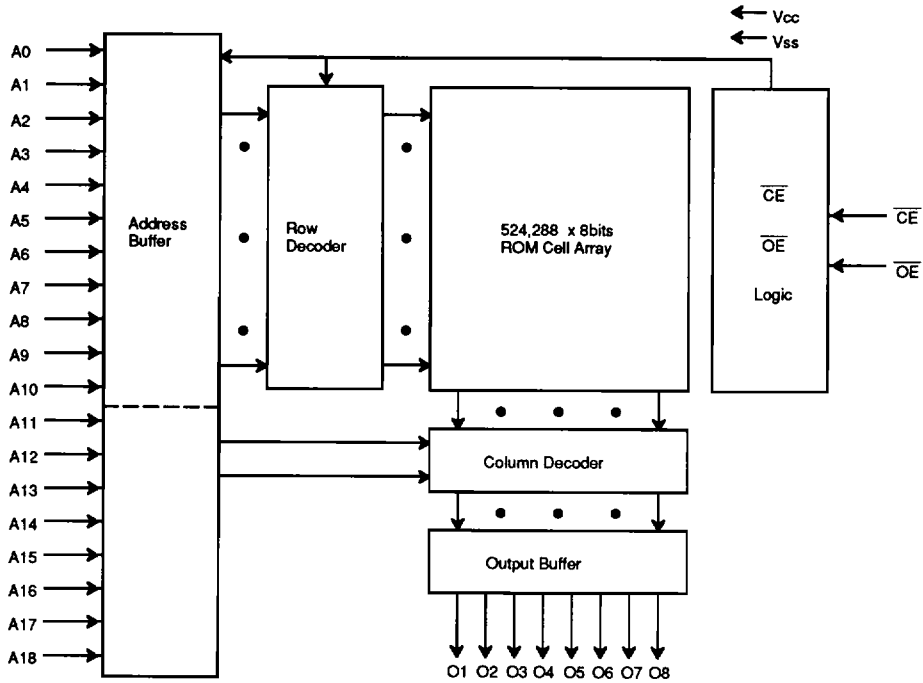
Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.3 to +7.0 *	V
Input Voltage	V _{IN}	-0.5 to V _{CC} +0.5 *	V
Output Voltage	V _{OUT}	-0.5 to V _{CC} +0.5 *	V
Temperature Under Bias	T _{BIAS}	-10 to +85	°C
Storage Temperature Range	T _{STG}	-45 to +125	°C

* Referenced to GND

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Fig. 1 — MB834000A BLOCK DIAGRAM



TRUTH TABLE

\overline{CE}	\overline{OE}	Mode	Output	Power Dissipation Mode
H	X	Not Selected	High-Z	Standby
L	H	Not Selected	High-Z	Active
L	L	Selected	D_{OUT}	Active

CAPACITANCE ($T_A=25^\circ C, f=1MHz$)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance ($V_{OUT}=0V$)	C_{OUT}			15	pF
Input Capacitance ($V_{IN}=0V$)	C_{IN}			10	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.3		0.8	V
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.3$	V
Ambient Temperature	T_A	0		70	°C

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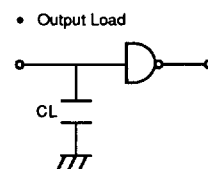
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Active Supply Current	$\overline{CE}=V_L$, Minimum Cycle	I_{CC}			40	mA
Standby Supply Current	$\overline{CE}=V_{IH}$	I_{SB1}			1	mA
	$\overline{CE}=V_{CC}=V_{IH}$, $V_{IN}=GND$ or V_{CC}	I_{SB2}			50	μA
Input Leakage Current	$V_{IN}=0$ to V_{CC}	I_{LI}	-10		10	μA
Output Leakage Current	$\overline{CE}=V_{IH}$, $\overline{OE}=V_{IH}$	$I_{L/O}$	-10		10	μA
Output High Voltage	$I_{OH}=-400\mu A$	V_{OH}	2.4			V
Output Low Voltage	$I_{OL}=2.1mA$	V_{OL}			0.4	V

Fig. 2 — AC TEST CONDITIONS

- Input Pulse Level : 0.6 to 2.4V
- Input Pulse Rise and Fall Time : $t_r=5ns$
- Timing Reference Levels : Input: $V_{IL}=0.8V$, $V_{IH}=2.2V$
Output: $V_{OL}=0.8V$, $V_{OH}=2.2V$
- Output Load : 1 TTL Gate and 100pF



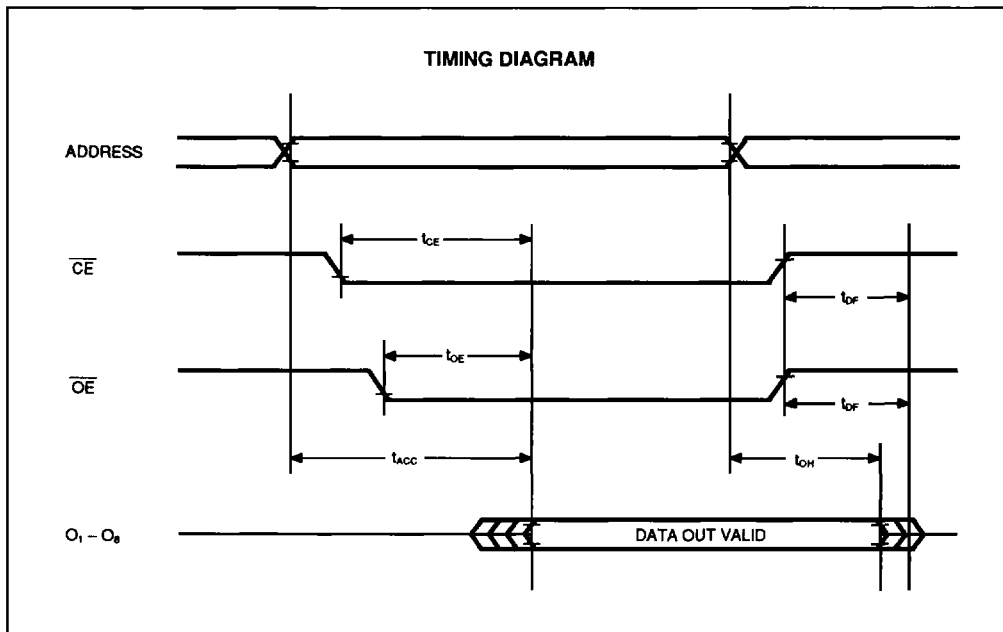
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	t_{ACC}		200	ns
Chip Enable Access Time	$\overline{OE}=V_{IL}$	t_{CE}		200	ns
Output Enable Access Time	Note 1	t_{OE}		80	ns
Output Disable Time	Note 2	t_{OF}		60	ns
Output Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	t_{OH}	0		ns

Note 1: Maximum \overline{OE} delay which does not affect t_{ACC} is $t_{ACC} - t_{OE}$.

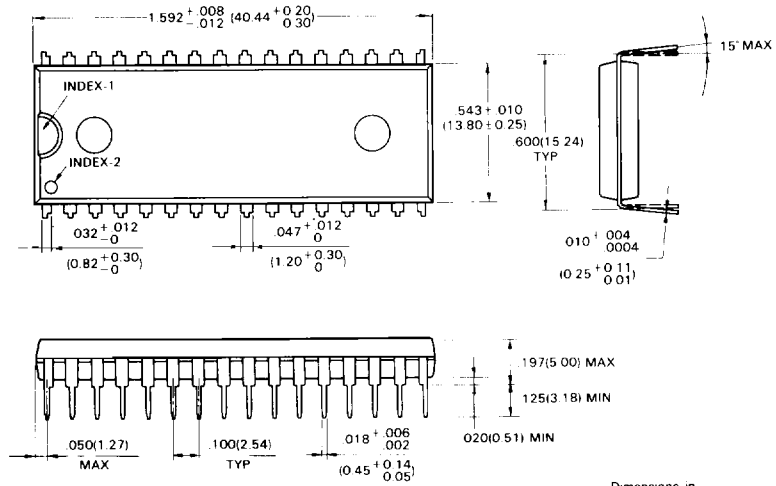
Note 2: t_{OF} is specified by either of \overline{CE} or \overline{OE} changing to High earlier.



PACKAGE DIMENSIONS

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32-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. DIP-32P-M01)



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Dimensions in inches (millimeters)

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