INTEGRATED CIRCUIT **TOSHIBA**

TECHNICAL DATA

TOSHIBA MOS INTEGRATED CIRCUIT TC5332202 AP SILICON GATE CMOS

32 MBIT (2,097,152 WORD BY 16 BITS) CMOS MASK ROM

DESCRIPTION

The TC5332202AP is a 33,554,432-bit Read Only Memory organized as 2,097,152 words by 16 bits. The TC5332202AP is most suitable for application such as program memory, data memory, and character generators.

The TC5332202AP is packaged in a standard 600 mil 42-pin DIP.

FEATURES

Single 5 V Power Supply

Access Time: 120 ns (max)

Power Dissipation

Operating Current: 45 mA (max) Standby Current: 100 \(\mu A \) (max) Fully Static Operation

• All Inputs and Outputs: TTL Compatible

• Three State Outputs

• TC5332202AP: DIP42-P-600

PIN ASSIGNMENT (TOP VIEW)

A18 🛚	1	\bigcup	42	A19
A17 [2		41	_ A8
A7 🛭	3		40	∆9
A6 [4		39	_ A10
A5 🛭	5		38	A11
A4 [6		37	A12
A3 [7		36	A13
A2 [8		35	A14
A1 [9		34	A15
A0 [10		33	_ A16
CE [11		32	BYTE
GND [12		31	GND
OE [13		30	D15
D0 [14		29	<u> </u> D7
D8 🛚	15		28	D14
D1 🛭	16		27	₫ D6
D9 [17		26	D13
D2 🛭	18		25	D5
D10 [19		24	D12
D3 [20		23	D4
D11 [21		22	D VDD
				J

TC5332202AP

PIN NAMES

A0 to A20	Address Inputs
D0 to D15	Data Outputs
CE	Chip Enable Input
ŌĒ	Output Enable Input
V _{DD}	Power Supply
GND	Ground

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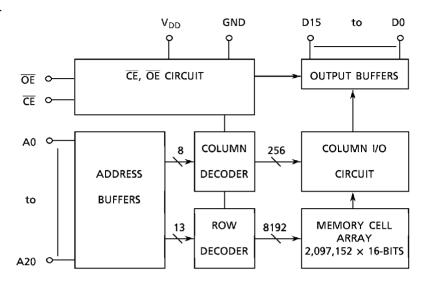
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BLOCK DIAGRAM



MODE SELECTION

MODE	CE	ŌĒ	D0 to D15	POWER
Read (16-Bit)	L	L	Data Out	Active
Output Deselect	L	Н	High Impedance	Active
Standby	Н	*	High Impedance	Standby

H: V_{IH} L: V_{IL} *: V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	- 0.5 to 7.0	٧
V _{IN}	Input Voltage	- 0.5 to 7.0	V
V _{OUT}	Output Voltage	0 to V _{DD} + 0.5	V
P _D	Power Dissipation	0.6	W
T _{STG}	Storage Temperature	- 55 to 150	°C
T _{OPR}	Operating Temperature	- 10 to 70	°C
T _{SOLDER}	Soldering Temperature (10 s)	260	°C

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DC RECOMMENDED OPERATING CONDITIONS (Ta = - 10° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	٧
V _{IH}	Input High Voltage	2.2	-	V _{DD} + 0.5	٧
V _{IL}	Input Low Voltage	- 0.3	_	0.8	V

DC CHARACTERISTICS (Ta = -10° to 70° C, $V_{DD} = 5 \text{ V} \pm 10\%$)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
I _{IL}	Input Leakage Current	$V_{IN} = 0$ to V_{DD}	-	± 5.0	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0 to V _{DD}	-	± 5.0	μΑ
Іон	Output High Current	V _{OH} = 2.4 V	- 1.0	-	mA
I _{OL}	Output Low Current	V _{OL} = 0.4 V	2.0	-	mA
I _{DD\$1}	Chandles Course	CE = V _{IH}	-	2	mA
I _{DD\$2}	Standby Current	$\overline{CE} = V_{DD} - 0.2 V$	-	100	μΑ
I _{DDO1}	Operating Current	$V_{IN} = V_{IH}/V_{IL}$, $t_{cycle} = 120 \text{ ns}$ $I_{OUT} = 0 \text{ mA}$	-	50	mA
I _{DDO2}	Operating Current	$V_{IN} = V_{DD} - 0.2 \text{ V/0.2 V}$ $t_{cycle} = 120 \text{ ns, } I_{OUT} = 0 \text{ mA}$	_	45	mA

CAPACITANCE (f = 1 MHz, Ta = 25° C, $V_{DD} = 5.0 \text{ V}$)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C _{IN}	Input Capacitance	$V_{IN} = 0 V$	-	15	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0 V	_	15	pF

Note: This parameter is periodically sampled and is not tested for every component.

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AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = -10° to 70° C, $V_{DD} = 5 \text{ V} \pm 10\%$)

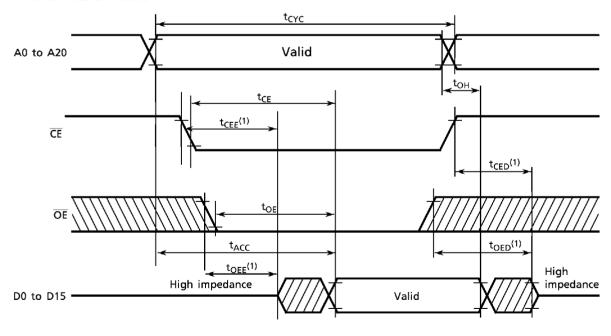
SYMBOL	PARAMETER	MIN	MAX	UNIT
t _{CYC}	Cycle Time	120	_	ns
t _{ACC}	Address Access Time	_	120	ns
t _{CE}	Chip Enable Access Time	_	120	ns
t _{OE}	Output Enable Access Time	_	60	ns
t _{CEE}	Output Enable Time from CE	0	_	ns
t _{OEE}	Output Enable Time from OE	0	-	ns
t _{CED}	Output Disable Time from CE	_	45	ns
t _{OED}	Output Disable Time from $\overline{\text{OE}}$	_	35	ns
t _{OH}	Output Hold Time	5	_	ns

AC TEST CONDITIONS

Output Load : 100 pF + 1 TTLInput Levels : $0.6\,\mathrm{V}/2.4\,\mathrm{V}$ Timing Measurement Reference Levels Input : 0.8 V/2.2 V

Output: 0.8 V/2.2 V Input Rise and Fall Time : 5 ns

16-BIT READ MODE



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