

TTL ISOPLANAR MEMORY 93411/93411A

256×1—BIT FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION — The 93411 and 93411A are high-speed 256-bit TTL Random Access Memories with full decoding on chip. They are organized 256 words by one bit and are designed for scratchpad, buffer and distributed main memory applications. The devices have three chip select lines to simplify their use in larger memory systems. Address input pin locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. An uncommitted collector output is provided to permit "OR-ties" for ease of memory expansion.

- REPLACEMENT FOR 54/74S206 AND EQUIVALENT DEVICES
- ORGANIZATION — 256 WORDS X 1 BIT
- THREE HIGH-SPEED CHIP SELECT INPUTS
- TYPICAL ACCESS TIME

93411A	Commercial	40 ns
93411	Commercial	45 ns
93411	Military	45 ns
- ON CHIP DECODING
- POWER DISSIPATION — 1.8 mW/BIT
- POWER DISSIPATION DECREASES WITH TEMPERATURE
- INVERTED DATA OUTPUT

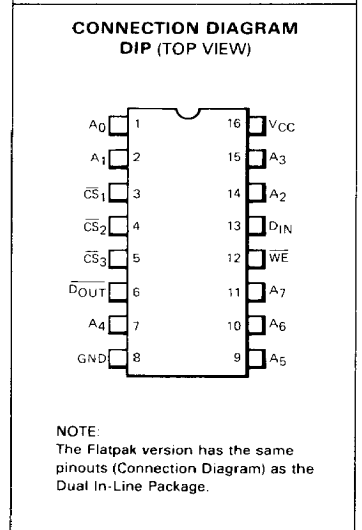
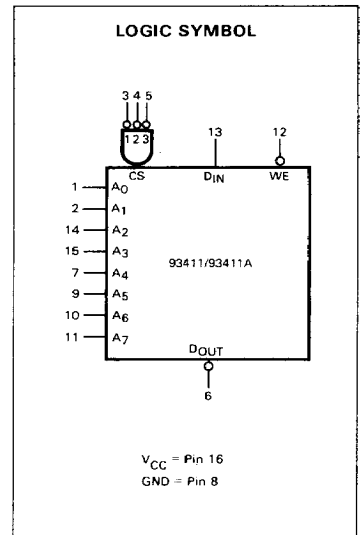
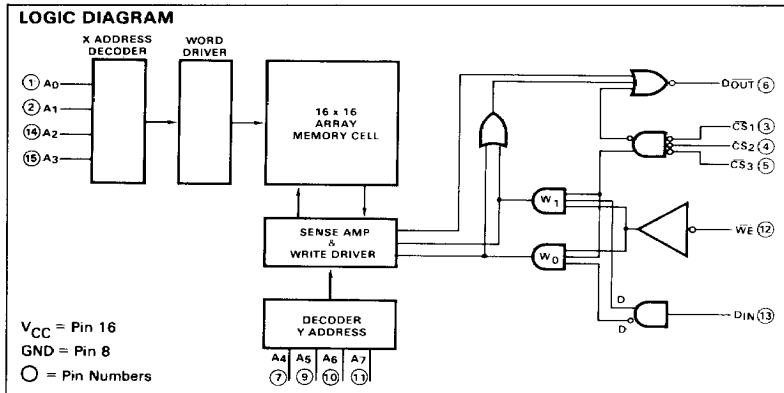
PIN NAMES

$\overline{CS}_1, \overline{CS}_2, \overline{CS}_3$	Chip Select Inputs	0.5 U.L.
A ₀ — A ₇	Address Inputs	0.5 U.L.
D _{IN}	Data Input	0.5 U.L.
\overline{D}_{OUT}	Data Output	10 U.L.
WE	Write Enable	0.5 U.L.

LOADING
(Notes a, b)

NOTES:

- a. 1 Unit Load (U.L.) = 40 μ A HIGH / 1.6 mA LOW
- b. 10 U.L. is the output LOW drive factor. An external pull-up resistor is needed to provide HIGH level drive capability. This output will sink a maximum of 16 mA at $V_{OUT} = 0.45$ V.



FAIRCHILD ISOPLANAR TTL MEMORY • 93411/93411A

FUNCTIONAL DESCRIPTION — The 93411/93411A are fully decoded 256-bit Random Access Memories organized 256 words by one bit. Word selection is achieved by means of an 8-bit address, A₀ through A₇.

Three Chip Select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select, \overline{CS} , from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable (\overline{WE} , pin 12). With \overline{WE} held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, \overline{WE} is held HIGH and the chip selected. Data in the specified location is presented at \overline{D}_{OUT} .

Uncommitted collector outputs are provided to allow maximum flexibility in output connection. In many applications, such as memory expansion, the outputs of several 93411s or 93411As can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of value R_L must be used to provide a HIGH at the output when it is off. Any value of R_L within the range specified below may be used.

$$\frac{V_{CC}(\text{MAX})}{16 - \text{F.O. (1.6)}} \leq R_L \leq \frac{V_{CC}(\text{MIN}) - V_{OH}}{n(I_{CEX}) + \text{F.O. (0.04)}}$$

R_L is in kΩ
 n = number of wired-OR outputs tied together
 F.O. = number of TTL Unit Loads (U.L.) driven
 I_{CEX} = Memory Output Leakage Current in mA
 V_{OH} = Required Output HIGH level at Output Node

The minimum value of R_L is limited by output current sinking ability. The maximum value of R_L is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.

TABLE I — TRUTH TABLE

INPUTS					OUTPUT	MODE
\overline{CS}_1 PIN 3	\overline{CS}_2 PIN 4	\overline{CS}_3 PIN 5	\overline{WE}	D _{IN}	\overline{D}_{OUT}	
H	X	X	X	X	H	Not Selected
X	H	X	X	X	H	Not Selected
X	X	H	X	X	H	Not Selected
L	L	L	L	L	H	Write "0"
L	L	L	L	H	H	Write "1"
L	L	L	H	X	\overline{D}_{OUT}	Read inverted data from addressed location

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care (HIGH or LOW)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V _{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	-0.5 V to +5.50 V
Output Current (dc) (output LOW)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
 **Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V _{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93411AXC, 93411XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93411XM	4.50 V	5.0 V	5.50 V	-55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.



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DC CHARACTERISTICS: Over Operating Temperature Ranges. Notes 1, 2 and 4

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX		
V _{OL}	Output LOW Voltage		0.3	0.45	V	V _{CC} = MIN, I _{OL} = 16 mA
V _{IH}	Input HIGH Voltage	2.0	1.6		V	Guaranteed Input Logical HIGH Voltage for all Inputs
V _{IL}	Input LOW Voltage		1.5	0.85	V	Guaranteed Input Logical LOW Voltage for all Inputs
I _{IL}	Input LOW Current		-530	-800	μA	V _{CC} = MAX, V _{IN} = 0 V
I _{IH}	Input HIGH Current		1.0	20	μA	V _{CC} = MAX, V _{IN} = 4.5 V
I _{CEX}	Output Leakage Current		1.0	50	μA	V _{CC} = MAX, V _{OUT} = 4.5 V
V _{CD}	Input Clamp Diode Voltage		-1.0	-1.5	V	V _{CC} = MAX, I _{IN} = -10 mA
I _{CC}	Power Supply Current	93411XC	90	124	mA	V _{CC} = MAX, WE Grounded, all other inputs @ 4.5 V, see Power Supply vs Temp. Curve
		93411AXC	100	135		
		93411XM	90	117		
			100	143		

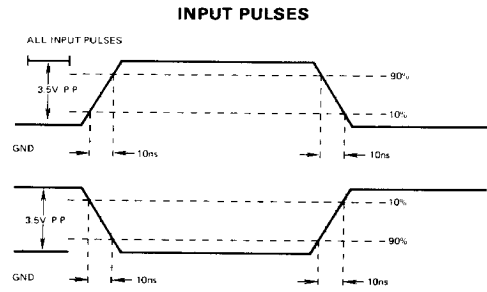
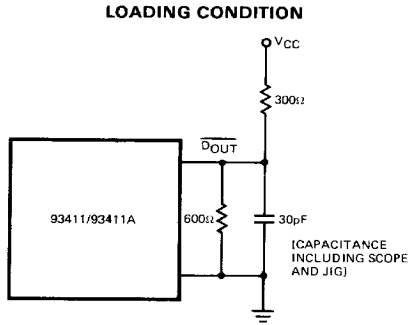
AC CHARACTERISTICS: Over Guaranteed Operating Ranges. Notes 1, 2, 4, 5, 6

SYMBOL	CHARACTERISTIC	93411AXC			93411XC			93411XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES											
t _{ACS}	Chip Select Time		25	30		25	30		25	40	ns	See Test Circuit and Waveforms Note 5
t _{RCS}	Chip Select Recovery Time		25	25		25	25		25	35		
t _{AA}	Address Access Time		40	45		45	55		45	65		
WRITE MODE	DELAY TIMES											
t _{WS}	Write Disable Time	10	20	35	10	20	35	10	20	45	ns	
t _{WR}	Write Recovery Time		25	40		25	40		25	50		
	INPUT TIMING REQUIREMENTS											
t _W	Write Pulse Width (to guarantee write)	40	25		40	25		50	25		ns	See Test Circuit and Waveforms Note 6
t _{WSD}	Data Set-Up Time Prior to Write	0	0	0	0	0	0	0	0	0		
t _{WHD}	Data Hold Time After Write	5	0	5	0	5	0	5	0	0		
t _{WSA}	Address Set-Up Time	0	0	0	0	0	0	0	0	0		
t _{WHA}	Address Hold Time	5	0	5	0	5	0	5	0	0		
t _{WSCS}	Chip Select Set-Up Time	0	0	0	0	0	0	0	0	0		
t _{WHCS}	Chip Select Hold Time	5	0	5	0	5	0	5	0	0		
C _I	Input Lead Capacitance		4	5		4	4		4	5		
C _O	Output Lead Capacitance		7	8		7	8		7	8		

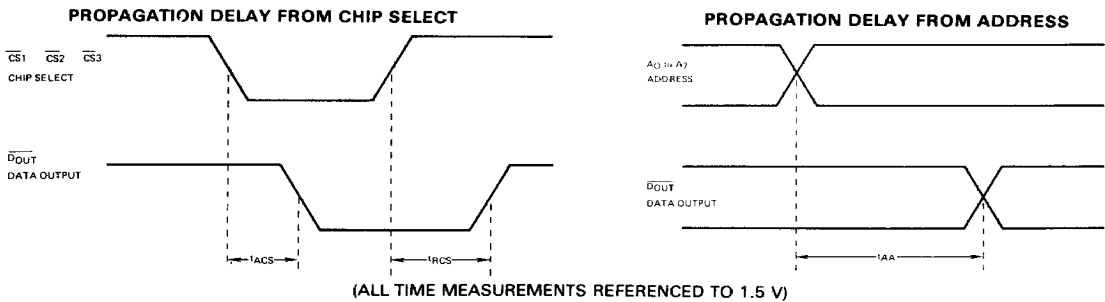
NOTES:

- Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
- The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
- Typical values are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
- The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:
 θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
 θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
 θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.
- The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
- t_W measured at t_{WSA} = MIN, t_{WSD} measured at t_W = MIN.

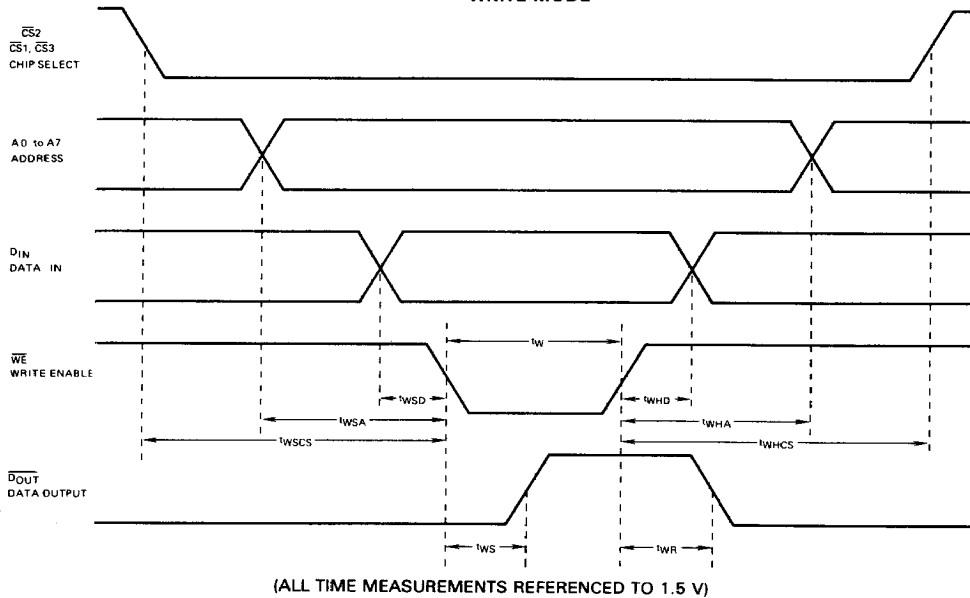
AC TEST LOAD AND WAVEFORM



AC WAVEFORMS
READ MODE



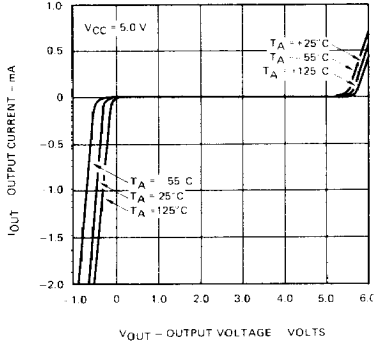
WRITE MODE



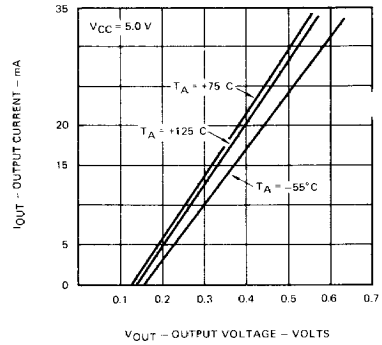
NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

TYPICAL ELECTRICAL CHARACTERISTICS

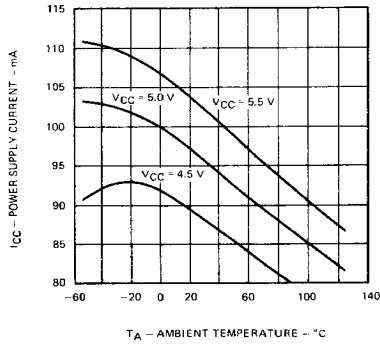
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



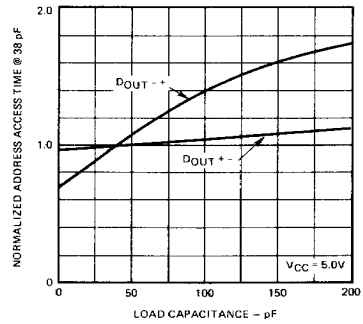
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



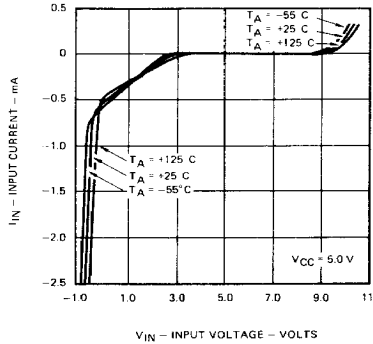
POWER SUPPLY CURRENT VERSUS TEMPERATURE



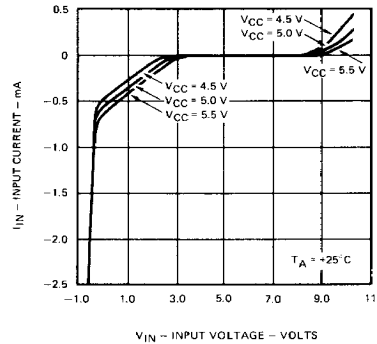
NORMALIZED ADDRESS ACCESS TIME VERSUS LOAD CAPACITANCE



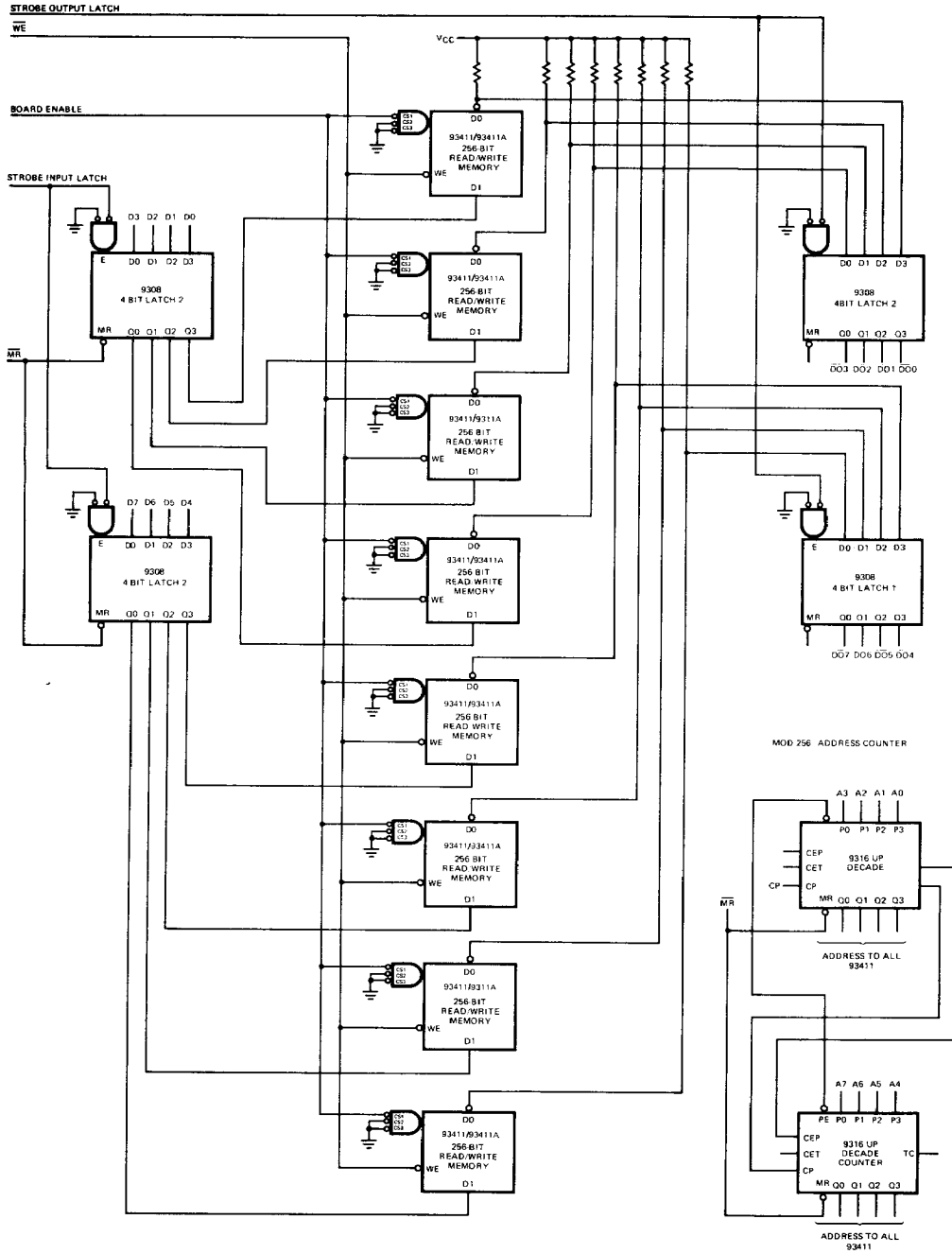
INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE



INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS SUPPLY VOLTAGE



APPLICATIONS



256-WORD BY 8-BIT BUFFER MEMORY SYSTEM