

FEATURES

- Very High Speed - 20, 25, 30 ns (Max.)
- **Fast output enable (tOE) for cache applications**
- Automatic power-down when chip is deselected
- CMOS Low Power Operation
 - 400mW (Typical) Operating
 - 55mW (Typical) Standby
 - 25µW (Typical) Power-down
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation-no clock refresh required
- Three state outputs
- Two chip enables ($\overline{CE1}$ and $\overline{CE2}$) for simple memory expansion
- Data retention as low as 2V for battery back-up

DESCRIPTION

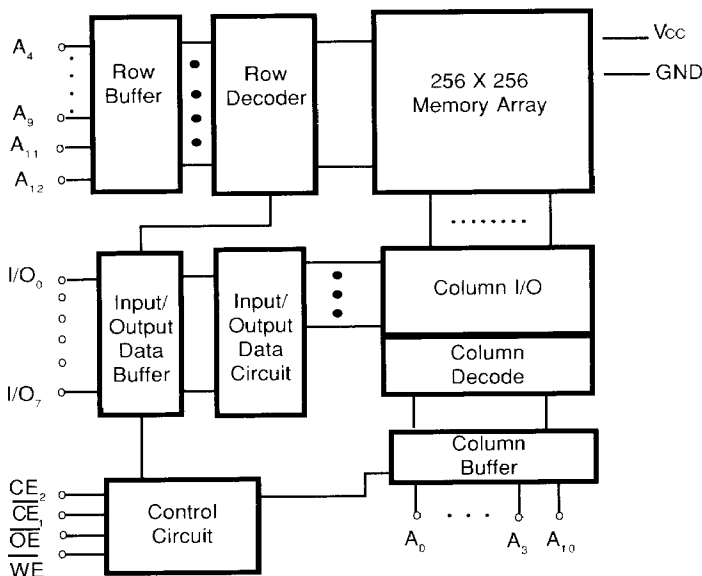
The ISSI IS61C64 is a very high speed, low power, 8192 words by 8 bit static RAM. It is fabricated using ISSI's high performance CMOS double metal technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 20ns with low power consumption.

When $\overline{CE1}$ is high or $\overline{CE2}$ is low (de-selected), the device assumes a standby mode at which the power dissipation can be reduced down to 25µW (typical) with CMOS input levels.

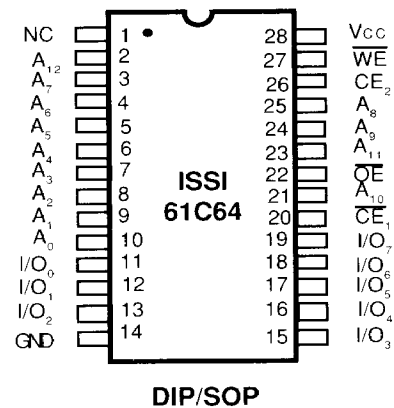
Easy memory expansion is provided by using two chip Enable Inputs, $\overline{CE1}$ and $\overline{CE2}$. The active low Write Enable (\overline{WE}) controls both writing and reading of the memory.

The IS61C64 is packaged in the JEDEC standard 28 pin, 600mil DIP, the space saving 300mil DIP and SOP surface mount packages.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



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IS 61C64

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

SYMBOL	PARAMETER	VALUE	UNIT
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC output Current (low)	20	mA

OPERATING RANGE

Range	Ambient Temperature	V _{CC}
Commercial	0°C to 70°C	5V ±10%
Industrial	-40°C to 85°C	5V ±10%

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics over Operating Range

Parameters	Description	Test Conditions	IS61C64-S20		IS61C64-S25		IS61C64-S30		Units
			IS61C64-L20		IS61C64-L25		IS61C64-L30		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{OH}	Output High Voltage	V _{CC} = MIN., I _{OH} = -4.0mA	2.4		2.4		2.4		V
V _{OL}	Output Low Voltage	V _{CC} = MIN., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input High Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input Low Voltage (2)		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{CC}	-10	10	-10	10	-10	10	µA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled	-10	10	-10	10	-10	10	µA
I _{OS}	Output Short Circuit Current (1)	V _{CC} = MAX., V _{OUT} = GND		100		80		65	mA
I _{CC1}	V _{CC} Operating Supply Current (3)	V _{CC} = MAX., I _{OUT} = 0mA, f = 0		140		120		105	mA
I _{CC2}	V _{CC} Dynamic Operating Supply Current (3)	V _{CC} = MAX., I _{OUT} = 0 mA, f = f _{MAX.}		170		145		125	mA
I _{SB1}	TTL Standby Current (TTL Inputs) (3)	V _{CC} = MAX., V _{IN} = V _{IH} OR V _{IL} CE1 ≥ V _{IH} OR CE2 ≤ V _{IL} , f = 0		30		25		20	mA
I _{SB2}	CMOS Standby Current (CMOS Inputs) (3)	V _{CC} = Max., CE1 ≥ V _{CC} - 0.2V CE2 ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V, OR V _{IN} ≤ 0.2V, f = 0	S	5	S	4	S	3	mA
			L	100	L	100	L	100	µA

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. V_{IL} = -3.0V for pulse width less than 10ns.
3. AT f=f_{max} address and data input are cycling at the maximum frequency, f=0 means no input lines change.

Capacitance (1,2)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	5	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	7	pF

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: TA= 25°C, f=1MHz, V_{CC}=5.0V

TRUTH TABLE

MODE	\overline{WE}	\overline{CE}_1	CE_2	\overline{OE}	I/O OPERATION	V_{CC} CURRENT
Not Selected (Power Down)	X	H	X	X	High Z	I_{SB_1}, I_{SB_2}
	X	X	L	X	High Z	I_{SB_1}, I_{SB_2}
Output Disabled	H	L	H	H	High Z	I_{CC_1}, I_{CC_2}
Read	H	L	H	L	DOUT	I_{CC_1}, I_{CC_2}
Write	L	L	H	X	DIN	I_{CC_1}, I_{CC_2}

Switching Characteristics Over Operating Range (1)

Parameters	Description	IS61C64-S20 IS61C64-L20		IS61C64-S25 IS61C64-L25		IS61C64-S30 IS61C64-L30		Units
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE								
t _{RC}	Read Cycle Time	20		25		30		ns
t _{AA}	Address Access Time		20		25		30	ns
t _{OHA}	Output Hold Time	3		3		3		ns
t _{ACE1}	\overline{CE}_1 Access Time		20		25		30	ns
t _{ACE2}	CE_2 Access Time		20		25		30	ns
t _{DOE}	\overline{OE} Access Time		7		9		12	ns
t _{LZOE}	\overline{OE} to Low Z Output	0		0		0		ns
t _{HZOE(2)}	\overline{OE} to High Z Output		7		9		12	ns
t _{LZCE1}	\overline{CE}_1 to Low Z Output	3		3		3		ns
t _{LZCE2}	CE_2 to Low Z Output	3		3		3		ns
t _{HZCE(2)}	\overline{CE}_1 or CE_2 to High Z Output		10		12		15	ns
t _{PU}	\overline{CE}_1 or CE_2 to Power Up	0		0		0		ns
t _{PD}	\overline{CE}_1 or CE_2 to Power Down		20		20		20	ns
WRITE CYCLE (3)								
t _{WC}	Write Cycle Time	20		25		30		ns
t _{SCE1}	\overline{CE}_1 to Write End	17		22		25		ns
t _{SCE2}	CE_2 to Write End	17		22		25		ns
t _{AW}	Address Set-up Time to Write End	15		20		25		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-up Time	0		0		0		ns
t _{PWE (4)}	\overline{WE} Pulse Width	12		15		18		ns
t _{SD}	Data Set-up to Write End	10		12		15		ns
t _{HD}	Data hold from Write End	0		0		0		ns
t _{HZWE (2)}	\overline{WE} Low to High-Z Output		10		12		15	ns
t _{LZWE}	\overline{WE} High to Low-Z Output	0		0		0		ns

Notes:

1. Test conditions assume signal transition times of 5ns or less, timing reference levels of 1.5V, Input pulse levels of 0 to 3.0V and output loading specified in figure 1a.
2. Tested with the load in Figure 1b. Transition is measured $\pm 500mV$ from steady state voltage.
3. The internal write time is defined by the overlap of \overline{CE}_1 low, CE_2 high and \overline{WE} low. All signals must be in valid states to initiate a Write, but anyone can go inactive to terminate the Write. The Data input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. Tested with \overline{OE} high.
5. \overline{WE} is high for a Read Cycle.
6. The device is continuously selected. $\overline{OE}, \overline{CE}_1 = V_{IL}, CE_2 = V_{IH}$.
7. Address is valid prior to or coincident with \overline{CE}_1 Low and CE_2 High transitions.
8. I/O will assume the High-Z state if $\overline{OE}=V_{IH}$.

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AC TEST CONDITIONS

Input Pulse Level	0 V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing and Reference Level	1.5V

AC TEST LOADS

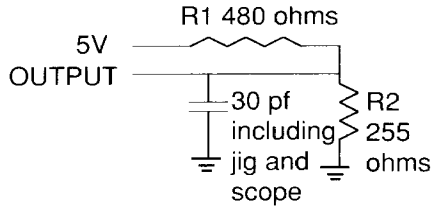


Figure 1a

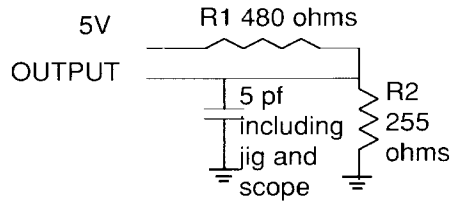
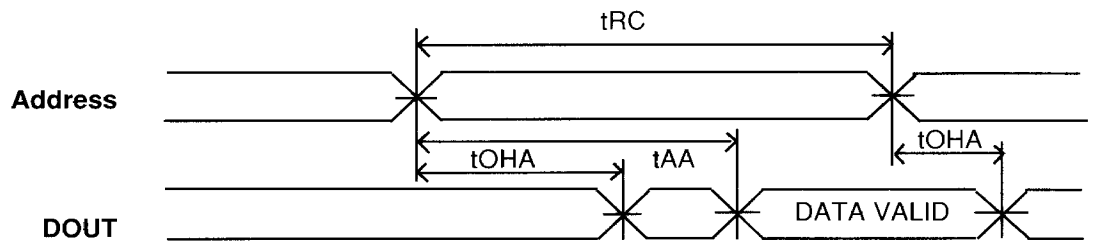


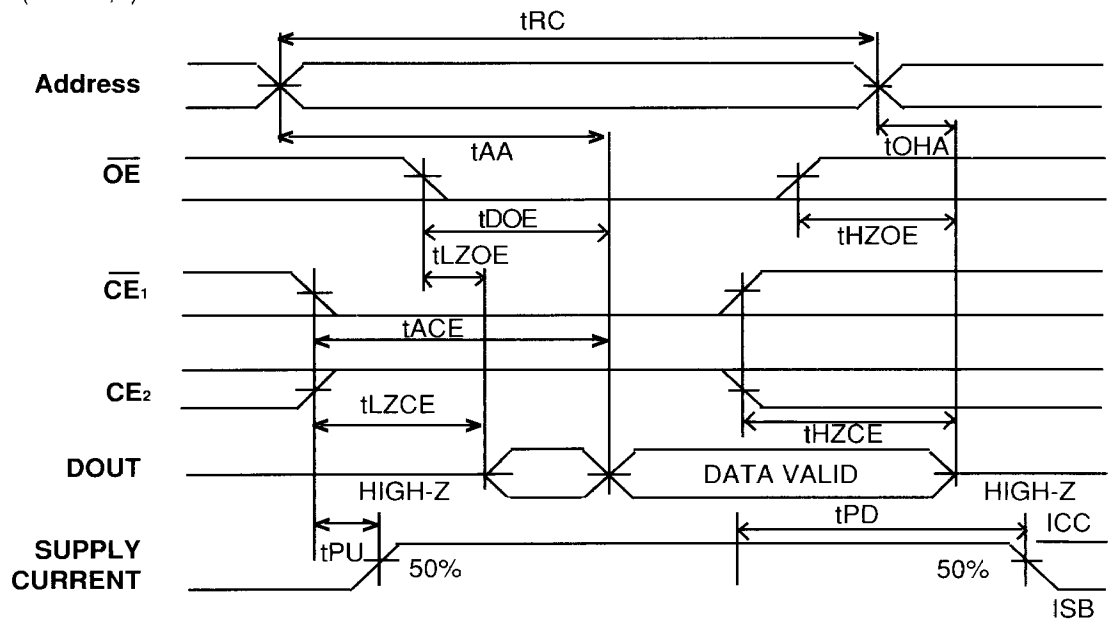
Figure 1b

AC WAVEFORMS

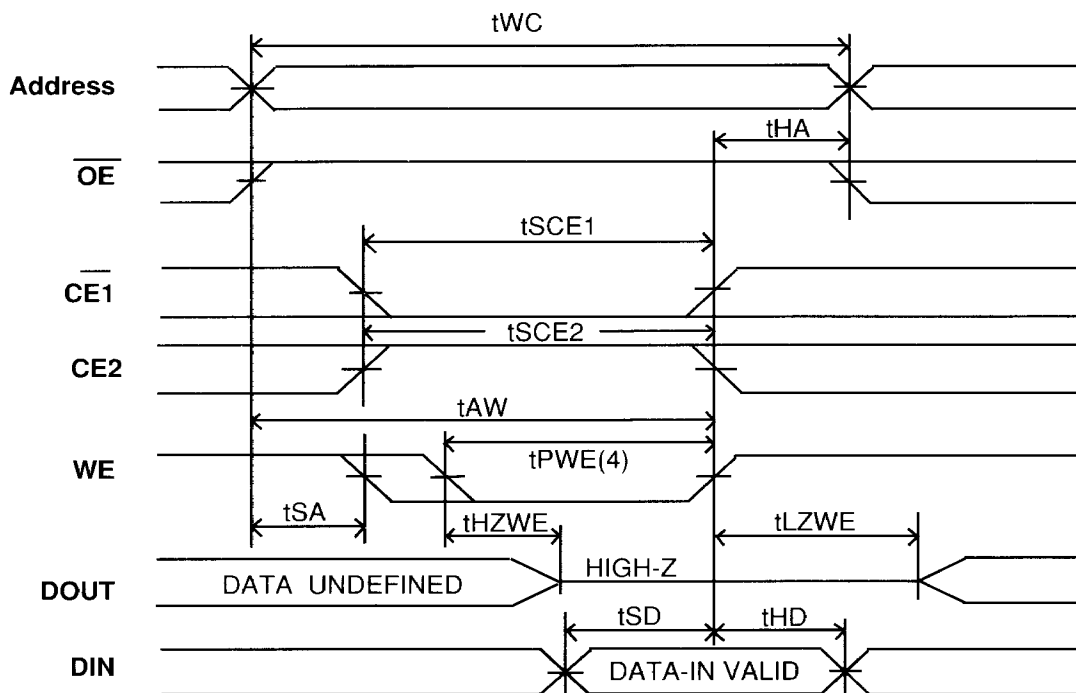
READ CYCLE NO. 1 (Note 5,6)



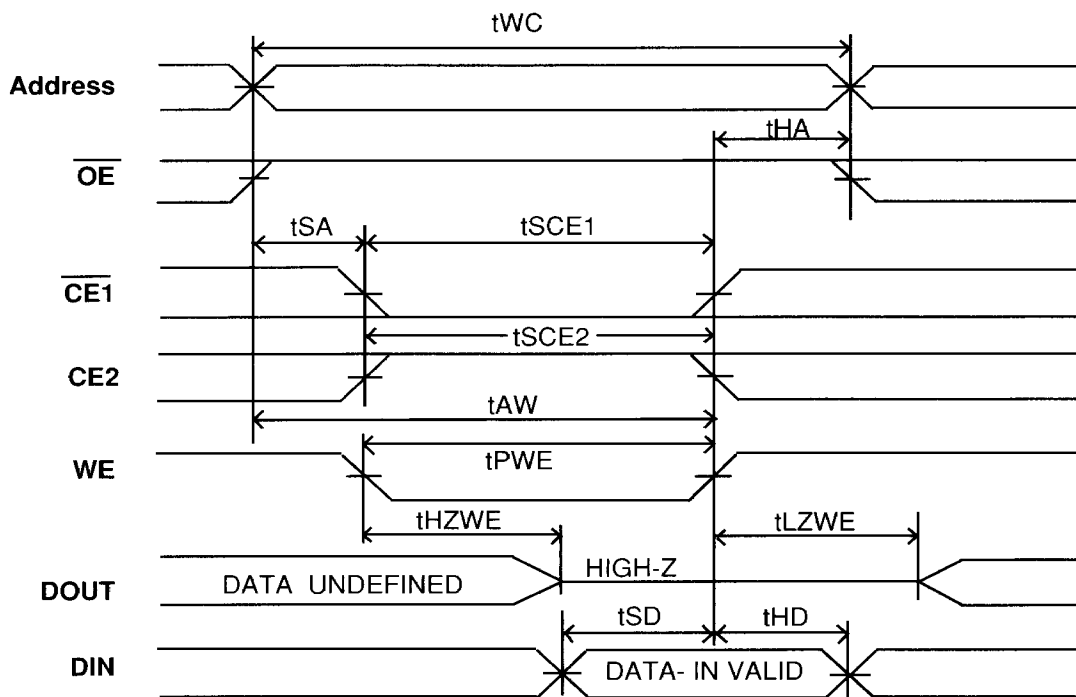
READ CYCLE NO. 2 (Note 5,7)



WRITE CYCLE NO. 1 (\overline{WE} controlled) (Note 3,8)



WRITE CYCLE NO. 2 ($\overline{CE1}$, $\overline{CE2}$ controlled) (Note 3,8)

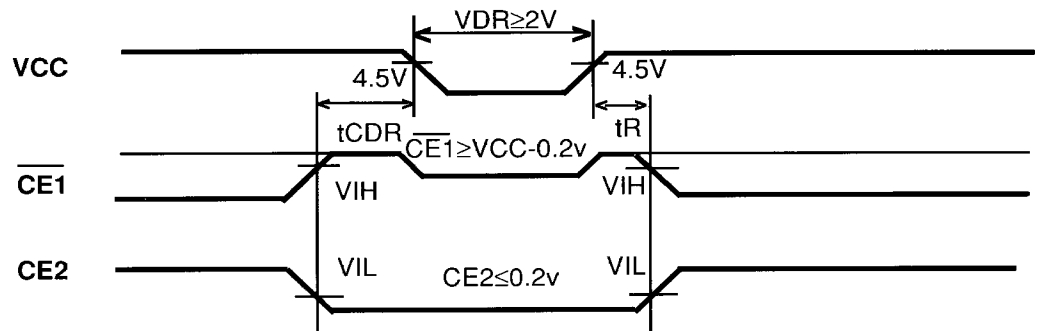


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DATA RETENTION CHARACTERISTICS (L Version only)

Parameter	Description	Test Condition	Min.	Max.	Units
VDR	VCC for retention of data	VCC = 2.0V	2.0	----	V
ICCDR	Data retention current	CE1 ≥ VCC - 0.2V,	-----	100	μA
tCDR	Chip deselect to data retention time	CE2 ≤ 0.2V,	0	-----	ns
tR	Operation recovery time	CMOS Inputs	tRC	----	ns
ILI	Input leakage current		-----	2	μA

DATA RETENTION WAVEFORM



PIN DESCRIPTIONS

$A_0 - A_{12}$ Address Inputs

These 13 address inputs select one of the 8192 8-bit words in the RAM.

$\overline{CE1}$ Chip Enable 1 Input

CE2 Chip Enable 2 Input

CE1 is active Low and CE2 is active High. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

\overline{OE} Output Enable Input

The output enable input is active Low. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the I/O pins and they will be enabled. The I/O pins will be in the high-impedance state when OE is inactive.

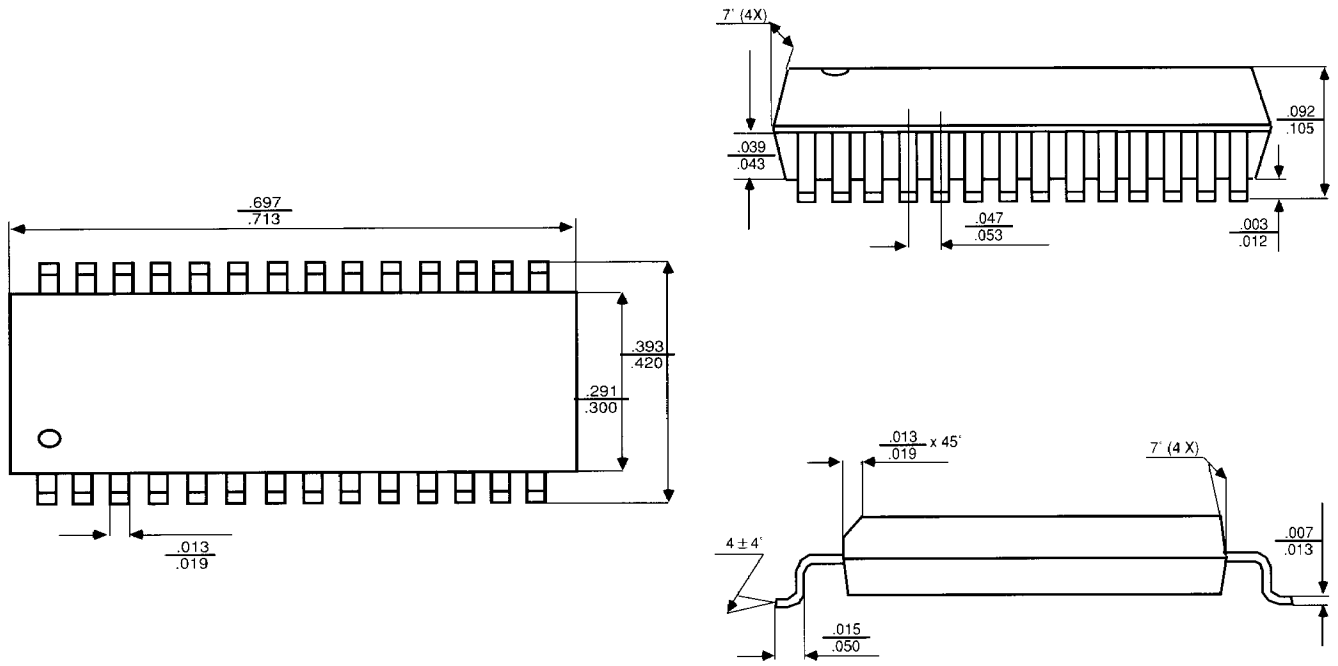
\overline{WE} Write Enable Input

The write enable input is active Low and controls read and write operations. With the chip selected, when \overline{WE} is Low Input data present on the I/O pins will be written into the selected memory location.

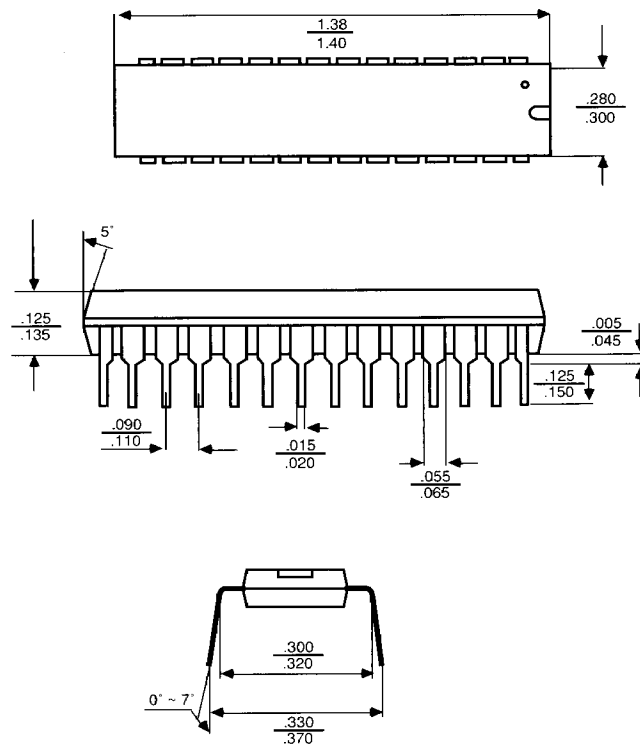
$I/O_0 - I/O_7$

These 8 bidirectional ports are used to read data from or write data into the RAM.

SOP Package Type

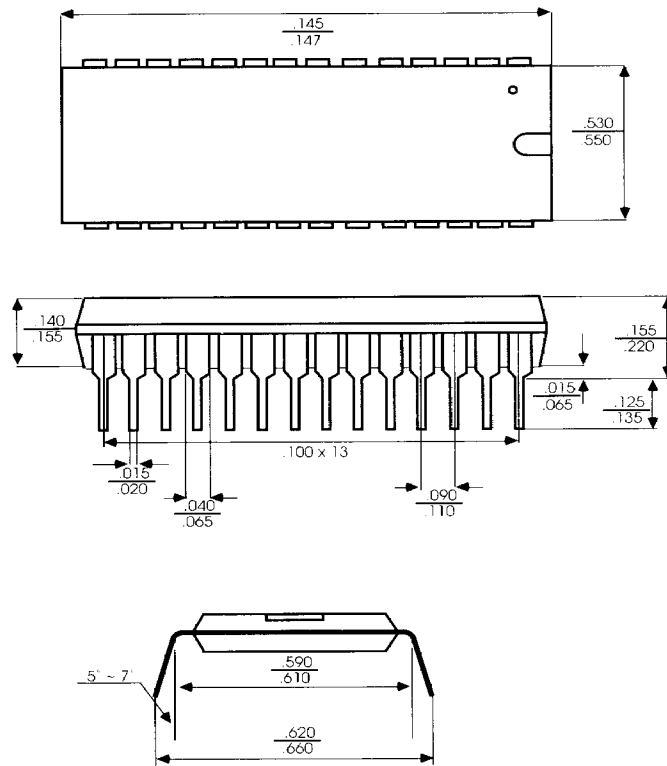


300 MIL Plastic Dip Package Type



IS 61C64

600 MIL Plastic Dip Package Type



SPEED (ns)	ORDER PART NUMBER	PACKAGE	TEMPERATURE RANGE
20	IS61C64-S20N	Plastic DIP - 300 mil	0°C to +70°C
20 STD.	IS61C64-S20P	Plastic Small Outline	0°C to +70°C
20	IS61C64-S20W	Plastic DIP - 600 mil	0°C to +70°C
20	IS61C64-L20N	Plastic DIP - 300 mil	0°C to +70°C
20 LOW	IS61C64-L20P	Plastic Small Outline	0°C to +70°C
20 POWER	IS61C64-L20W	Plastic DIP - 600 mil	0°C to +70°C
25	IS61C64-S25N	Plastic DIP - 300 mil	0°C to +70°C
25 STD.	IS61C64-S25P	Plastic Small Outline	0°C to +70°C
25	IS61C64-S25W	Plastic DIP - 600 mil	0°C to +70°C
25	IS61C64-L25N	Plastic DIP - 300 mil	0°C to +70°C
25 LOW	IS61C64-L25P	Plastic Small Outline	0°C to +70°C
25 POWER	IS61C64-L25W	Plastic DIP - 600 mil	0°C to +70°C
30	IS61C64-S30N	Plastic DIP - 300 mil	0°C to +70°C
30 STD.	IS61C64-S30P	Plastic Small Outline	0°C to +70°C
30	IS61C64-S30W	Plastic DIP - 600 mil	0°C to +70°C
30	IS61C64-L30N	Plastic DIP - 300 mil	0°C to +70°C
30 LOW	IS61C64-L30P	Plastic Small Outline	0°C to +70°C
30 POWER	IS61C64-L30W	Plastic DIP - 600 mil	0°C to +70°C

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